a third semiconductor layer of said second conductivity type higher in an impurity concentration and thinner than said second semiconductor layer, and provided on a surface of said second semiconductor layer;

a fourth semiconductor layer of said first conductivity type provided on a surface of said third semiconductor layer, wherein said third semiconductor layer is interposed between said second semiconductor layer and a bottom of said fourth semiconductor layer and is in direct contact with said second semiconductor layer;

Delete.

a fifth semiconductor layer of the second conductivity type selectively provided in a surface of said fourth semiconductor layer and opposing said third semiconductor layer through said fourth semiconductor layer;

a first main electrode disposed across and connected with surfaces of said fourth and fifth semiconductor layers;

a second main electrode provided on said second main surface of said first semiconductor layer;

an insulating film provided on a portion of said fourth semiconductor layer interposed between said third and fifth semiconductor layers; and

a control electrode facing said portion through said insulating film so that said portion

1 2 last forms a channel region as an only channel region of said insulated gate semiconductor device.

REMARKS

Favorable reconsideration of this application, in view of the following comments and as presently amended, is respectfully requested.